Remarks

Favorable reconsideration of this application is requested in view of the following remarks. For the reasons set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The non-final Office Action dated June 17, 2003, indicated that the proposed drawings were approved; claims 1-4 and 7-10 are rejected under 35 U.S.C. § 102(a) over *Berthoumieux et al.* (European Patent No. 0 447 302); and claims 5, 6 and 11-28 are rejected under 35 U.S.C. § 103(a) over *Berthoumieux et al.* in view of *Krasner* (U.S. Patent No. 5,841,396).

With respect to the drawings, Applicant will submit formal drawings including the proposed drawing corrections submitted in the December 2002 Office Action Response once the instant application is allowed.

Applicant respectfully traverses each of the prior art rejections and respectfully submits that each of the rejections is deficient for failing to present a *prima facie* case of correspondence between the claimed invention and the cited prior art, considering the *Berthoumieux* reference alone or in combination with the *Krasner* reference. Under Section 103(a), the claimed invention must be considered "as a whole" and, therefore, with all its limitations. *See, e.g.*, MPEP § 2143.03. However, contrary to the law, the rejections of the claims are based on unsupported assertions of anticipation/obviousness with express acknowledgements that the cited prior art fails to teach important aspects of the claimed invention. In connection with these rejections, Applicant submits that, by merely asserting conclusions of such prior art teaching, without evidentiary support, a good portion of the claimed limitations after the transition phrase (*e.g.*, "comprising") have been ignored.

For example, the Office Action acknowledges that the *Berthoumieux* reference fails to teach the aspects of the claimed invention directed to effectively disabling the analog circuitry from its data processing tasks. These acknowledgements are discussed in Office Action paragraphs, No. 24 (regarding the last subparagraph of claim 11), No. 36 (regarding the last subparagraph of claim 18), and No. 42 (regarding the respective last subparagraphs of claims 23 and 24). Other (express and implied) acknowledgements of prior art deficiencies are exemplified by way of the claimed first and second communication

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intervals and the first (reduced activity) and second (other) communication modes, as first introduced by claim 1. At paragraph No. 10, the Office Acton appears to acknowledge that the *Berthoumieux* reference does not teach the claimed other communication mode during which the shorter time interval occurs. In connection with this rejection, the Office Action does not attempt to correlate the cited prior art with the claimed modes and intervals. Moreover, the *Berthoumieux* reference teaches merely a first regular-communication operation and another reduced-activity operation in which there is no communication mode. Reference may be made to the examples discussed beginning at the bottom of page 3 of the *Berthoumieux* reference.

Another example is in connection with the Examiner's distorted attempts to equate "guard time" as "when a signal is neither being received nor transmitted." *See, e.g.*, Office Action at paragraph Nos. 12 and 47. While in this instance the Office Action attempts to correlate the cited prior art with the claimed "guard" term, the Office Action completely ignores the surrounding claim terms. In connection with claims 2-27, for instance, the Office Action and the *Berthoumieux* reference are devoid of the claimed aspects: "during a known guard time for the data being communicated to the communication arrangement." Again, the *Berthoumieux* reference teaches merely a first regular-communication operation and another reduced-activity operation in which there is no communication mode. It is untenable to argue that the claimed aspect, "during a known guard time for the data being communicated to the communication arrangement", corresponds to any period in which no data is being communicated to the communication arrangement. Reference may be made to the examples discussed beginning at the bottom of page 3 of the *Berthoumieux* reference.

Because each of the above independent claims includes limitations that are not taught by the cited prior art (taken alone or in combination), the rejections are improper, and the Section 103(a) rejections cannot be maintained. Accordingly, Applicant requests that the rejection be removed.

With particular respect to the rejection of claim 8, the Office Action is plainly wrong in asserting that the data written to the memory is inherently asynchronous to the rate at which data is read from memory due to differing operating speeds of the digital and analog components. This unsupported Office Action assertion contradicts

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conventional circuit operation having a divide-by clock circuit that generates synchronous clock signals from a single clock source where each synchronous clock signal is a multiple of the other. *See, e.g.*, U.S. Patent Nos. 5,457,456, 6,396,768, and 6,452,421. As evidenced herein, differing clock speeds do not inherently result in asynchronous data transmission. Rather, in order to establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991) (emphasis added). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.* at 1269, 20 U.S.P.Q.2d at 1749 (quoting *In re Oelrich*, 666 F.2d 578, 581, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981). The Office Action fails to provide any of the requisite evidence in support of the inherency assertion. Further, this assertion of inherency fails as the evidence clearly shows that if one of the digital or analog clocks operates at twice (or any multiple thereof) the speed of the other clock, the data will likely still be synchronous. Accordingly, the inherency argument is unsupported, incorrect and therefore cannot be maintained.

Regarding the rejection of claims 9 and 10, the Office Action's assertion that the memory can be read from and written to by both the analog and digital circuitry because the device both receives and transmits data is also both unsupported and plainly incorrect. As outlined above, the Office Action fails to present the requisite evidence to support such an inherency argument. Further, the memory circuit would clearly not be able to be read from and written to by both the analog and digital circuitry if the memory included two memory circuits, one for transmitting to and one for receiving from as is common in processing arrangements. Accordingly, the inherency argument is unsupported, incorrect and therefore cannot be maintained.

With respect to the rejection of claims 5, 6 and 11-28, in which the combined teachings of *Berthoumieux* and *Krasner* are relied upon, in addition to the prior-art correspondence issues discussed above, the Office Action fails to appreciate that the time control component 4 of *Berthoumieux* only responds and reacts to instants when data is

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being received and processed by the ADC 5; therefore, the proposed modification based on *Krasner* would not permit for disabling of the ADC 5 without entirely undermining the objective and operation of *Berthoumieux*. Applicant's response in this regard was addressed previously and the instant Office Action provided no substantive response; rather, the Office Action merely restated a generic point in the law: a point that has nothing to do with Applicant's argument that the proposed modification would undermine the purpose and operation of *Berthoumieux*. See MPEP §2143.01. Pursuant to MPEP § 707.07(f), due to the failure to address Applicant's argument in a substantive manner, the § 103(a) rejection must be withdrawn. Thus, with Applicant's argument being ignored, under MPEP § 707.07(f) and MPEP §2143.01, the Section 103(a) rejection cannot be maintained.

Applicant further maintains its previously presented argument that each of the rejections is based on improper hindsight reconstruction directed at the claimed invention. None of the rejections cites any discussion in the prior art that would suggest the proposed combination. However, such evidence in the prior art is required in order to maintain a Section 103 rejection. As set forth in *Ruiz v. A.B. Chance Co.*, 234 F.3 654 (December 6, 2000), the alleged motivation for combining the references is to be suggested by the ***references*** themselves. As addressed above, the Office Action acknowledges that the prior art does not teach or suggest the claimed invention.

Please charge Deposit Account No. 50-0996 (STFD.005PA) in the amount of $42.00 for the additional independent claim and charge/credit the same Deposit Account No. for any deficiency/surplus.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance.

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Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at (651) 686-6633.

Respectfully submitted,

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Dated: September 22, 2003

By: Eric D. Curtis, Reg. No. 47,511, for
Robert J. Crawford
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